i960® Jx Microprocessor
The Cobra Series

Technical Overview

New Power/Performance Options for the i960 Processor Family

Since the i960® microprocessor family's introduction in 1988 with the i960 K series 32-bit embedded RISC microprocessors, Intel has added to the product line and now offers six commercial and two military versions of the architecture. The i960 C series processors have superscalar capabilities for embedded RISC devices. Averaging 30 design wins a month, the i960 architecture shipped more units, 4.6 million, in 1993 for embedded applications than all other RISC microprocessors combined*.

The i960 microprocessor family provides high-performance 32-bit embedded computing in versions ranging from less than $13, such as the i960 S series processors, to 100 MIPS, as in the i960 C series products. To continue offering customers increased performance, more integration and lower power devices, Intel has developed the Cobra series of the i960 architecture.

Initially, the Cobra series will include four parts, varying by cache sizes, core speeds and operating voltages.

The Cobra series processors are code-compatible with the existing i960 processor family members, including the i960 S series processors, which have a 16-bit external bus, the mid-range i960 K series processors, and the highest performance devices, the i960 C series processors.

FEATURES	80960 JD	80960 JF	80L960 JF	80L960 JA
100% K-Series Compatible System Bus	✔	✔	✔	✔
Scalar RISC Core	✔	✔	✔	✔
Two Integrated Timers	✔	✔	✔	✔
100% i960® C-Series processors Compatible Interrupt Controller	✔	✔	✔	✔
1K Byte Data RAM	✔	✔	✔	✔
4K Byte Instruction Cache	✔	✔	✔	
2K Byte Data Cache	✔	✔	✔	
2K Byte Instruction Cache				✔
1K Byte Data Cache				✔
5.0 V Operation	✔	✔		
3.3 V Operation			✔	✔
Speed Doubled Core	✔			

Table 1: i960® Jx Microprocessor, Cobra Series

**Source: Dataquest*

The Cobra processors target data-intensive embedded control tasks requiring efficient and fast data movement. Anticipated applications include enterprise networking devices, non-impact printers and intelligent I/O control.

Operating at 5 volts, i960 JD processor in the Cobra series will deliver 45 MIPS at 50 MHz to give system designers high-performance computing for low-power applications. Figure 1 compares the number of MIPS in comparison to other RISC microprocessors.

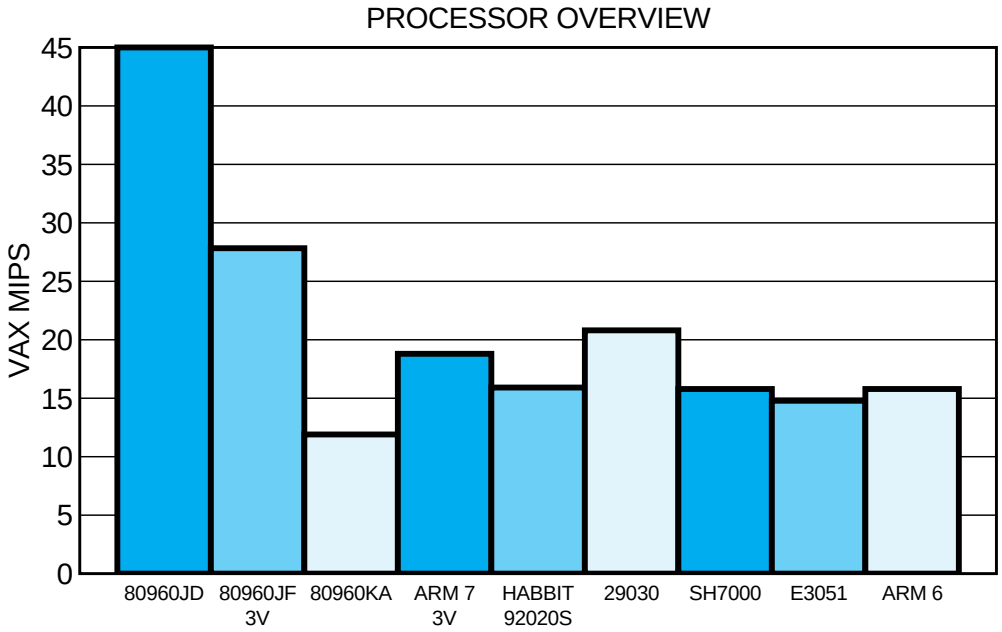

Figure 1: MIPS per Watt Comparison, i960® Jx Microprocessor

Enhancements to the existing i960 microprocessor family improve processor performance for the Cobra series while satisfying the requirements of low-power applications. New features and enhancements include:

- Improvements to the core microarchitecture
- Low power modes
- Local register cache
- New instructions
- Improved cache design
- Enhanced bus control unit
- Improved interrupt performance
- State-of-the-art testability
- Integrated peripherals

Core Microarchitecture Improvements

The i960 JD microprocessor is the first i960 microprocessor to incorporate Intel clock doubling technology. This technology enables the microprocessor to run at speeds up to 50 MHz internally while connecting to a lower-cost 25 MHz external system.

Clock doubling technology, which requires advanced semiconductor process technology, doubles the external system clock signal and provides the internal 2x clock signal to on-chip subunits.

A new, three-ported register file also represents an improvement to the microarchitecture. The three-ported register file provides a path to each of the three operands in the i960 architecture instructions. The multiple paths improve performance by reducing the contention to the internal operand source and destination buses.

The i960 Cobra processor block diagram, Figure 2, highlights many features and integrated peripherals found on all Cobra processors.

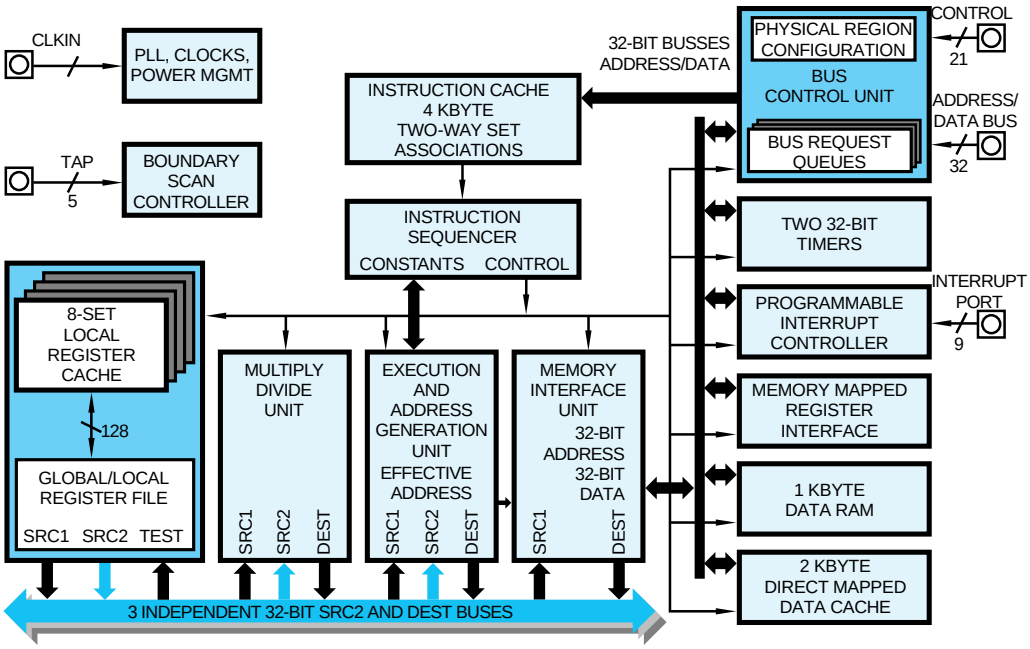

Figure 2: Cobra Series Block Diagram

In addition, the Cobra supports all combinations of register source and destination bypassing, a crucial factor in sustaining single-cycle per instruction RISC instructions. As with the current i960 C series processors, individual register scoreboarding is supported allowing concurrent instruction execution between the execution-unit (EU), multiply-divide-unit (MDU) and load/store operations.

Low Power Support

Many future designs in office equipment will support low-power operation, requiring the system to detect and initiate this mode. The system must reduce power in particular units of the equipment while maintaining the ability to return to normal operation — without physically restarting the system. New systems also will be required to use less power in normal operation.

The Cobra processors support a power-down mode of operation that reduces the power consumption by approximately 90 percent. Execution of the **HALT** instruction initiates a semi-sleep mode. During this mode, normal on-chip timer operation, support for external bus masters through the HOLD/HOLDA interface, and the ability to detect interrupts remains functional. The interrupt source can be from either an external device or the integrated timers. Once an interrupt occurs, the processor will "wakeup" and continue execution, starting with the instruction specified by the interrupt source.

To reduce power used in normal operation, the Cobra series is manufactured using .8 micron Intel process technology. The Cobra series processors can operate at either 5.0V or 3.3V voltages and are the first i960 processors in 3.3V versions.

Robust Register Set and Local Register Cache

Software performance has become increasingly critical in the embedded microprocessor environment. The i960 architecture includes a fast call-and-return mechanism to support the modular software base found in applications such as internetworking and imaging. The local register cache provides storage for the local registers availableto the software applications. At any time, an executing program has access to sixteen 32-bit local registers, and sixteen 32-bit global registers.

Software complexity for embedded control applications has forced embedded system designers to rely on high-level languages to develop applications. Structured high-level code requires a mechanism to save the state of an executing process when calling a procedure and to restore that state on return from the procedure. Typically, RISC architectures defer these tasks to the operating system, requiring multiple instructions to save the processor's state. Recognizing the frequent use of the call and return operation, the i960 architecture completely integrates this mechanism on-chip.

Flexibility to Add New Instructions

Software performance from RISC processors requires the CPU to reduce external bus traffic, executing instructions in a single cycle. The Cobra series microprocessors take this idea one more step. Instructions have been added to the i960 architecture, which offers significant flexibility, to enhance the Cobra series.

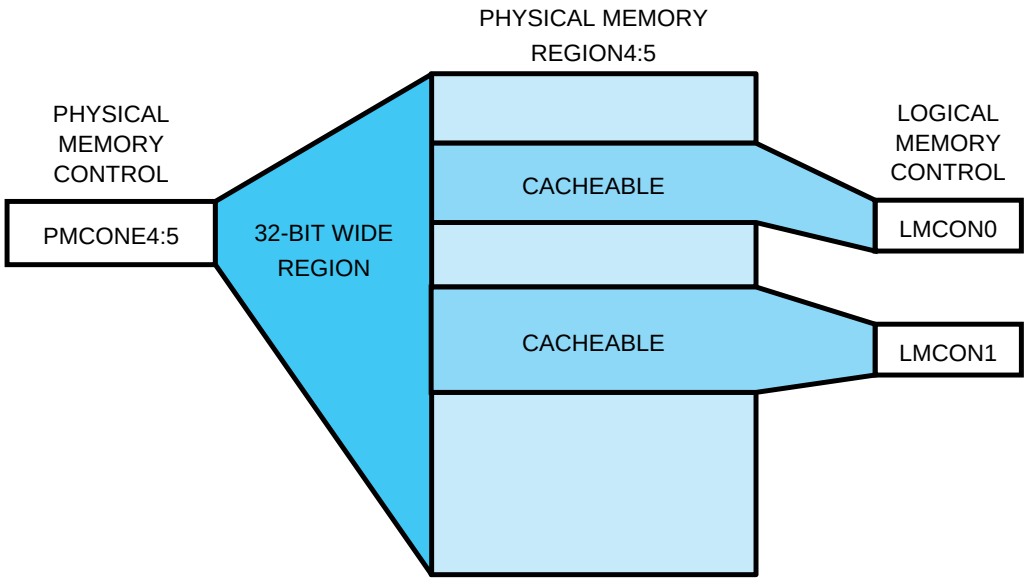

Figure 3: Logical Memory Control Example

For example, new instructions add flexibility to convert 32-bit word data from a little endian to big endian, or vice-versa. Cobra series processors can operate in either full little endian mode, or they can be configured in big endian mode.

Another added instruction, HALT, places the microprocessor in a reduced power operation.

Two instructions have been added to manipulate the caches, allowing programmers require the ability to probe the on-chip caches to refine software design, because on-chip caches have made programmers more sensitive to code structure and locality.

Advanced Cache Architecture

Processors in the Cobra series contain three independent caches: instruction cache, data cache, and local register cache. Besides the on-chip caches, there is a zero wait-state, on-chip data RAM.

The Cobra series processors provide a 2 Kbyte direct mapped data cache. The inclusion of a data cache is a significant performance enhancement for applications that keep most of their data in DRAM. A data cache also helps bus-intensive multi-master applications such as internetworking. While the processor accesses data in the internal caches, the memory bus is free for use by external agents such as Ethernet and Token Ring controllers.

The on-chip data RAM is a unique feature of the processor. A 1 Kbyte region of zero wait state memory provides storage for data variables and interrupt vectors. Unlike a data cache, variables can never be "kicked out" of the data RAM. Intel's compilers (CTOOLS960 and GNU960) can take advantage of the on-chip data RAM for critical variable storage, providing high speed and deterministic access to data.

Enhanced Bus Control Unit

The Cobra series bus control unit (BCU) adds functionality specifically for supporting data caches that have migrated on-chip and satisfies the needs of both the hardware designers and the software designers. Execution of code can occur on 32-, 16- or 8-bit external memory.

The local bus of the Cobra series processors is 100 percent compatible with the local bus found on the i960 K series processors. Additional pins provide additional information to the system hardware designers, supporting the "ease of system design" charter for all i960 microprocessors.

The i960 JD processor support both big and little endian data types. Hardware integrated into the BCU will automatically convert the data for big and little endian. There is also support for unaligned big or little endian data accesses.

Interrupt Performance

The Cobra series improves interrupt latency and throughput by supporting two operational modes: dedicated mode and expanded mode. Dedicated mode requires the external device to signal an interrupt request to the processor with a dedicated signal toggling. When the interrupt controller detects an active signal, it figures out the priority and vector of the associated interrupt. The dedicated mode of operation supports either edge or level detection besides fast or debounced sampling. Expanded mode requires the external device to place an interrupt vector on the interrupt pins, requiring the interrupt controller to read the pins and figure out the priority and vector of the interrupt.

The i960 JD processor also improves interrupt performance through other techniques:

- The processor core determines the address of the first instruction of the interrupt service routine from the priority vector. The Cobra series allows caching the interrupt vector addresses that point to the addresses of the first executable instruction. Reserved for this purpose are the first 64 bytes of on-chip data RAM. Caching these vectors reduces the external bus traffic, providing higher throughput.
- To reduce the time necessary for the processor to fetch the first instruction to be executed, the Cobra series processors can permanently lock critical sections of code, such as interrupt handlers in the instruction cache. The result: faster and more deterministic interrupt response time.

- The core performs a task switch to the interrupt service routine. This includes allocating a fresh register set, switching to a dedicated stack, and saving the previous internal state for later resumption of the underlying task. The Cobra series processors can reduce the task switch time reserving local register set(s) for interrupts priority 28 and higher.

These improvements enable the Cobra to reduce interrupt latency by a factor of five to 10 times the existing i960 K series microprocessors.

State-of-the-Art Testability

Enhancements include chip and system level testability, built-in self test, and on-chip breakpoint capabilities for software developers.

For example, the i960 JD processor integrates a built-in self test (BIST), which checks basic functionality of internal data paths, registers and memory arrays. All of the Cobra series processors support on-circuit emulation (ONCE) for board-level testing.

The Cobra series processors also support testability through the Test Access Port (TAP) controller, based on the IEEE 1149.1 (JTAG) standard Test Access Port and boundary scan architecture. The purpose of the TAP controller is to support the on-chip test logic such as built-in self-test, boundary-scan and scanout. The test logic unit is the gateway to all the test modes.

The increasing sizes of both instruction and data caches are reducing the number of external bus cycles, making it more difficult to figure out the actual software execution path. The Cobra series processors integrate on-chip hardware breakpoint registers to simplify the software develop-ment process. These hardware breakpoint registers consist of two instruction and two data address breakpoint registers. These registers work with the software debuggers such as Intel's DB-960 and GDB-960.

The Cobra series processors incorporate the latest technology to provide the necessary internal information to in-circuit emulators. The technology allows the processor to execute at 99.5 percent of the normal execution rate with the ICE operating in the system. This provides true, real-time debugging capability with full visibility into the processor.

Integrated Peripherals

The Cobra processors have integrated two major functions on-chip: an integrated timer unit and an integrated interrupt controller unit. Both units are highly flexible.

The integrated timer unit provides two identical 32-bit timers. The timers have a single shot mode and an auto-reload mode for continuous operation. Each timer has an independent interrupt request to the microprocessor interrupt controller. The timer registers interface through internal memory mapped addresses. When enabled, the timer control circuitry generates a fault when detecting unauthorized writes from user mode. The clocks for the system bus clock also clock the timers, allowing the timer clock frequency to remain consistent among the various proliferations within the i960 processor family.

The interrupt controller unit (ICU) provides a flexible, low-latency procedure for requesting interrupts. This unit handles the posting of interrupts requested by hardware and software sources. The interrupt controller, acting independently from the core, compares the priorities of posted interrupts with the current process priority, off-loading this task from the core. The interrupt controller provides the following features for handling hardware-requested interrupts:

- Support of up to 248 external sources
- Eight external interrupt pins
- One non-maskable interrupt pin
- Two internal timer sources for detection of hardware-requested interrupts
- Edge or level detection on external interrupt pins
- Debounce option on external interrupt pins.

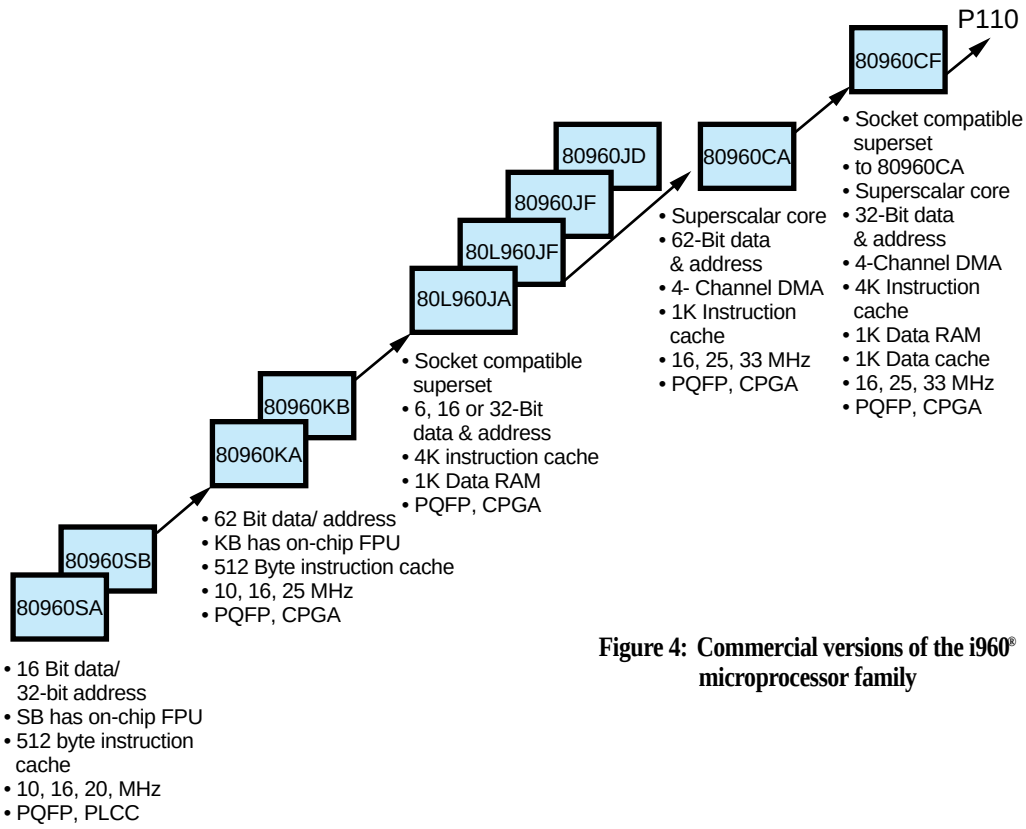

Figure 4: Commercial versions of the i960® microprocessor family

The i960 Architecture: Room To Grow

The i960 architecture provides implementations at widely varying price/performance points. Figure 4 illustrates the entire i960 family for commercial applications.

In summary, the four new versions of the Cobra series provide OEMs with low-power options, a host of new features to improve performance and testability, and new higher-performance options for embedded applications. The Cobra series are code-compatible with the existing i960 S, K and C series processors.

Support Information

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